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10/711,062	08/20/2004	Yen-Cheng Chen	AVIP0035USA	5061

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2622	

NOTIFICATION DATE	DELIVERY MODE
04/09/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/711,062	CHEN ET AL.	
	Examiner	Art Unit	
	NHAN T. TRAN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5 and 7-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5 and 7-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 5, 7-20 have been considered but are moot in view of the new ground of rejection.

Drawings

2. The replacement drawings of Figs. 1 & 2 were received on 1/24/2008 and accepted.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 9 & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brusewitz et al. (US 6,038,257) in view of Yamaguchi (EP 1 271 833).

Regarding claim 1, Brusewitz discloses an image-capturing apparatus with error-detecting function, the image-capturing apparatus (Fig. 1 and col. 7, lines 30-39) comprising:

a light sensor (indicated by camera 10) for sensing light reflected from an image and for transforming the light into an analog image signal (Fig. 1 and col. 2, lines 54-63);

an analog front-end device (subsampler 14 which is also analog to digital converter; see col. 3, lines 2-5) electrically connected to the light sensor for transforming the analog image signal into a digital image signal;

an encoder (16) for encoding the digital image signal (Fig. 1 and col. 3, lines 14-30);

a decoder (24) for decoding the encoded digital image signal encoded by the encoder (Fig. 1 and col. 4, lines 2-36);

a processor (22 in combination with 18) electrically connected to the decoder for determining whether the encoded digital image signal encoded by the encoder is correct or not (Fig. 1 and col. 7, lines 30-39);

a signal transmission device (20, 34) electrically connected between the light sensor, the decoder, and the processor for transmitting the encoded digital image signal encoded by the encoder and the control signal generated by the processor (Fig. 1 and col. 3, lines 59-66).

Brusewitz does not explicitly disclose a register electrically connected to the analog front-end device for storing the digital image transformed by the analog front-end device such that the encoder is electrically connected to the register for encoding the digital image signal stored in the register. Brusewitz is also silent as to the processor generates a control signal to control the encoder to re-encode the digital image signal

stored in the register when the processor determines that the encoded digital image signal encoded by the encoder is not correct.

However, in the same field of endeavor, Yamaguchi teaches an apparatus for transmitting images that includes a register (buffer 10 in Figs. 1 & 3) electrically connected to an analog front-end device (note that this analog front-end device is inherent in Yamaguchi's apparatus since the image data stored in buffer 10 is in digital format by virtue of data packet) for storing the digital image signal transformed by the analog front-end device (see Figs. 1 & 3 and paragraphs [0006] & [0031]). Yamaguchi also teaches an encoder (coding units 11 & 12) for encoding the digital image stored in the register (10) and transmitting the encoded image signal to a receiver (2). Yamaguchi further teaches that when an error in the encoded image is detected by an error detection unit (17), a retransmission information is issued by the receiver to control the encoder to re-encode the digital image stored in the register (10) and re-transmit the digital image to the receiver (see Figs. 1 & 3; paragraphs [0031]-[0035] & [0049]). Such implementation is to maintain high transmission efficiency while preventing delay time (see paragraph [0008]).

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Brusewitz and Yamaguchi to construct an imaging apparatus having a register electrically connected to the analog front-end device for storing the digital image transformed by the analog front-end device and the encoder electrically connected to the register for encoding the digital image signal stored in the register, and also configure the processor to generate a control signal to control the encoder to re-

encode the digital image signal stored in the register when the processor determines that the encoded digital image signal encoded by the encoder is not correct. Such implementation would maintain high transmission efficiency while preventing delay time as taught by Yamaguchi above.

Regarding claim 5, it is also seen from the combined teaching of Brusewitz and Yamaguchi that every time the analog front-end device transforms a new analog image signal into a new digital image signal, the analog front-end device updates the digital image signal stored in the register with the new digital image signal (see Fig. 1 in Brusewitz and Figs. 1 & 3 in Yamaguchi, wherein the new digital image inherently updates the buffer as it comes).

Regarding claim 9, the combined teaching of Brusewitz and Yamaguchi also discloses that the encoder, the decoder, and the processor form a cyclic-redundancy error-checking (CRC) mechanism (see Yamaguchi, col. 6, lines 12-13).

Regarding claim 16, Brusewitz discloses a camera (10) but silent as to the light sensor being a CCD. However, an Official Notice is taken that it is notoriously well known in the art to use CCD as an image sensor in a camera since the CCD provides high dynamic image output compared to other image sensor types.

For this reason, it would have been obvious to one of ordinary skill in the art to use CCD as the light sensor in Brusewitz.

5. Claims 7, 8, 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brusewitz et al. and Yamaguchi as applied to claim 1 and in further view of Johansson et al. (US 7,099,865).

Regarding claims 7 & 8, Brusewitz and Yamaguchi are just silent about the encoder, the decoder and the processor form an odd parity (or even parity) error-checking mechanism.

Johansson teaches that it is well known in the art to provide odd parity (or even parity) error-checking mechanism or cyclic redundancy error-checking (CRC) mechanism for a transmitting and receiving system for checking errors in transmitted data since these error-checking algorithms are popular and accurate so that the corrupted data due errors is replaced by requesting for a new data (see Johansson, col. 2, lines 28-36 and col. 5, line 30 – col. 6, line 14).

Therefore, it would have been obvious to one of ordinary skill in the art to provide an odd/even parity error-checking mechanism by the encoder, the decoder and the processor in Brusewitz and Yamaguchi in view of teaching of Johansson since the odd/even parity error-checking algorithm is one of the most popular and accurate method for checking errors in digital data.

Regarding claim 10, Brusewitz and Yamaguchi in view of Johansson as analyzed in claims 7 & 8 also encompasses that the digital image signal comprises N bits, and the encoded digital image signal encoded by the encoder from the digital image signal

comprises a check bit having a value set according to the N bits of the digital image signal and a predetermined error-checking mechanism formed according to the encoder, the decoder, and the processor, and N corresponding bit pairs, each of the bit pairs comprising an odd location bit and an even location bit equal to the odd location bit, and an odd location bit of an n^{th} bit pair of the encoded digital image signal having a value equal to that of an n^{th} bit of the digital image signal (see the analyses of claims 7 & 8 and Johansson in col. 5, lines 30-47, wherein the subject matter as claimed is inherently included in the odd/even or CRC error-checking mechanism).

Regarding claim 11, Brusewitz and Yamaguchi in view of Johansson as analyzed in claims 1 and 7-10 also discloses that the control signal is a null signal (when there is no error detected, see Yamaguchi, col. 6, lines 50-51).

Regarding claims 12-14, these claims are also met by the analyses of claims 7-9, respectively.

6. Claims 15, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brusewitz et al. and Yamaguchi and in further view of Poo et al. (US 2003/0005337).

Regarding claim 15, Brusewitz and Yamaguchi discloses all the subject matter as discussed in claim 1 but fails to explicitly disclose that the processor is an application-specific integrated circuit (ASIC).

However, as taught by Poo, an imaging system comprises a processor (10 in Fig. 1A) which is implemented by ASIC for processing output image from an imaging module (50) (see Poo, paragraph [0023]). It is also well understood by one skilled in the art that the application-specific integrated circuit would significantly reduce a number of circuit components, thereby reducing size and cost of overall circuitry in comparison to conventional non-integrated components.

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Brusewitz, Yamaguchi and Poo to make the processor as an application-specific integrated circuit for reducing size and cost of the imaging system.

Regarding claim 17, Brusewitz and Yamaguchi in view of Poo further discloses that the analog front-end device is installed in a light engine comprising the light sensor (see Poo, Fig. 1A, wherein the converter 54 is installed in the imaging module 50).

Regarding claim 18, Brusewitz and Yamaguchi in view of Poo further discloses that the encoder is installed in a light engine comprising the light sensor (see Poo, Fig. 1A).

Regarding claims 19 & 20, Brusewitz and Yamaguchi in view of Poo further discloses that the analog front-end device and the encoder are installed on a motherboard (see Poo, Figs. 1A in which all components are installed within the motherboard 70).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NHAN T. TRAN whose telephone number is (571)272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nhan T. Tran/
Primary Examiner, Art Unit 2622